**Cell Description:**This is a standard single-bit, positive-edge triggered flip-flop with an asynchronous, active low clear signal. The input signal to this cell is sampled on the rising edge of the clock signal, only the compliment of the sampled signal is available at the output of the cell.

**Truth Table:**

|  |  |  |  |
| --- | --- | --- | --- |
| **CLK** | **D** | **CLRBAR** |  |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 |  |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 |  |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 |

**Behavioral Verilog:**

//Verilog HDL for "Lib6710\_06", "DFF" "behavioral"

module DFFQB( QB, CLRB, CLK, D );

input CLRB;

input CLK;

input D;

output reg QB;

always@(posedge CLK or negedge CLRB) // Async clear

begin

if(~CLRB) //Active low clear

QB <= 1'b1;

else

QB <= ~D;

end

specify

(D => QB) = (1.0, 1.0);

(CLK => QB) = (1.0, 1.0);

(CLRB => QB) = (1.0, 1.0);

endspecify

endmodule

**Cell Size:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Height (μM)** | **Width (μM)** |
| DFFQBX1 | 27.0 | 48 |

**Performance:**

**Propagation Delay (Rising Outputs):**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
| DFFQBX1 |  |  |

**Propagation Delay (Falling Outputs):**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
| DFFQBX1 |  |  |

**Output Fall Time:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
| DFFQBX1 |  |  |

**Output Rise Time:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
| DFFQBX1 |  |  |

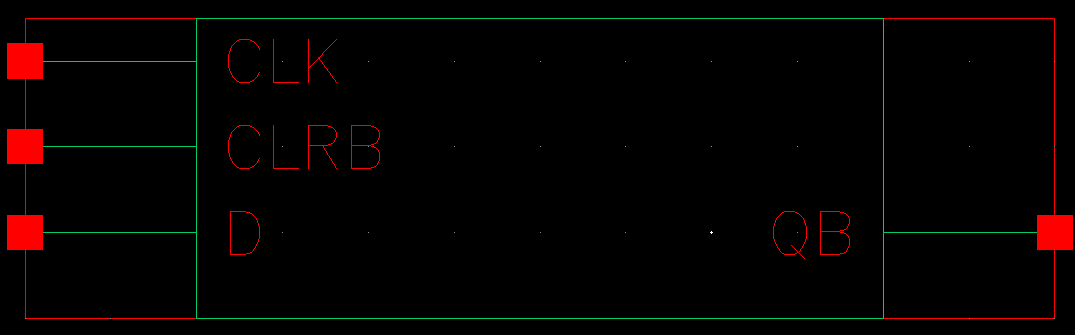
**Logic Symbol:  
**

Figure 1: Symbol View for the DFFQB cell.

**CMOS Schematic:**

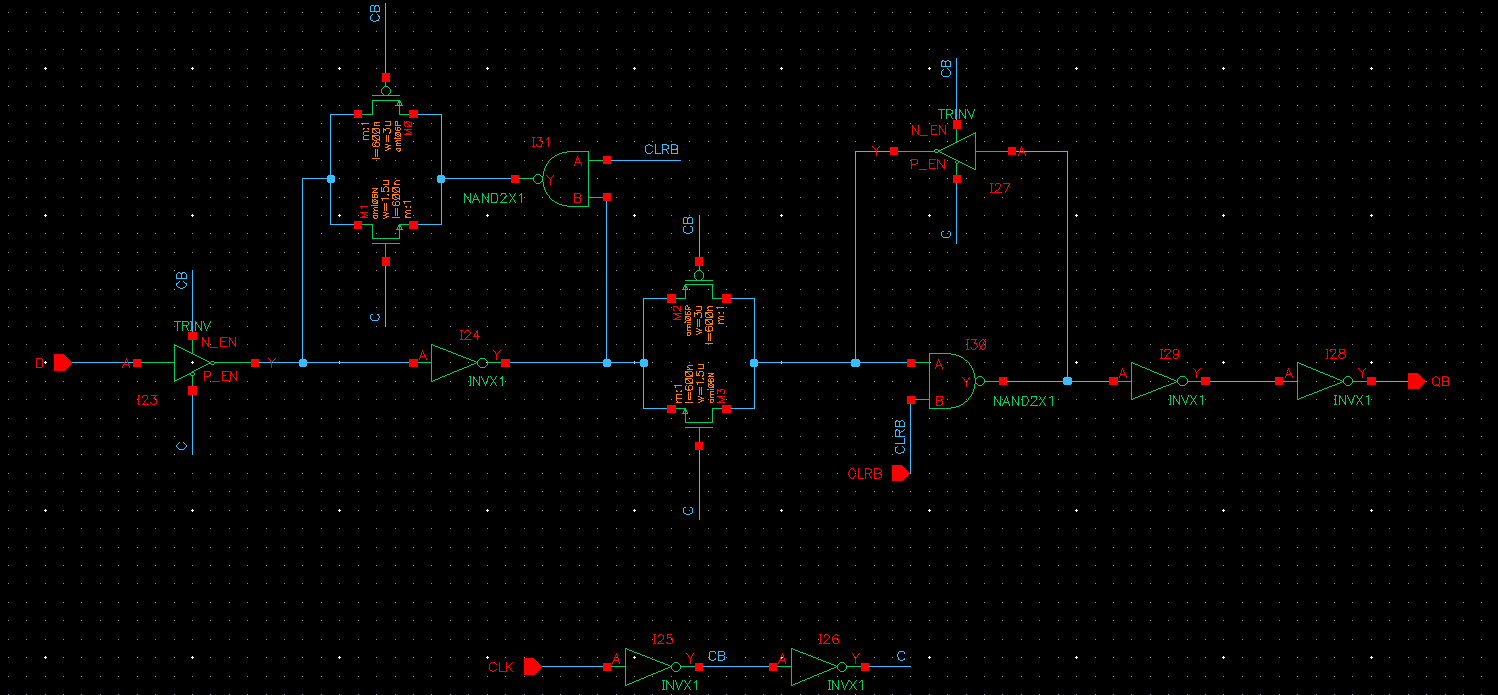
****

Figure 2: CMOS schematic for the DFFQBX1 Cell

**CMOS Layout:**

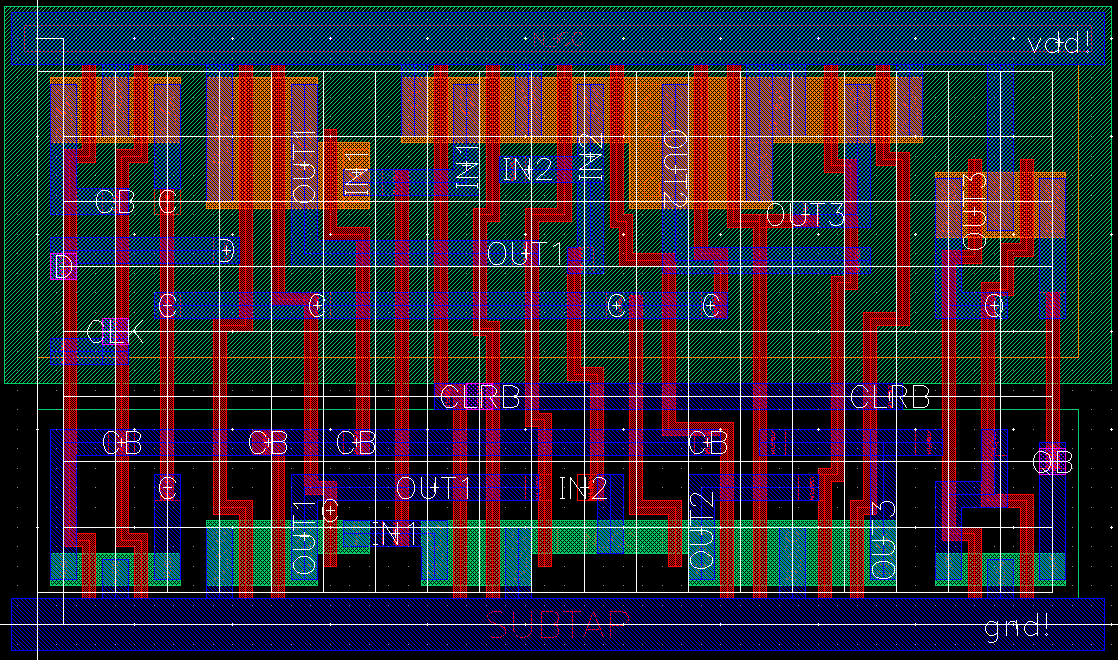
****

Figure 3: CMOS layout for the DFFQBX1 cell.